IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An interconnect substrate comprising:

a first substrate on which a first interconnect pattern is formed; and

a second substrate on which a second interconnect pattern is formed, wherein the first and second substrates are disposed so as to overlap each other but so as not to be in direct contact with each other;

at least one of the first interconnect pattern and the second interconnect pattern has a mounting region for an electronic chip; and

the first interconnect pattern and the second interconnect pattern are electrically connected by a conductive material therebetween.

2. (Currently Amended) The interconnect substrate as defined in claim 1, wherein:

the second substrate is larger than the first substrate, and

a whole surface of the first substrate is adhered to the second substrate by an adhesive material.

3. (Previously Presented) The interconnect substrate as defined in claim 1, wherein:

the first interconnect pattern is formed on a first surface of the first substrate;

the second interconnect pattern is formed on a second surface of the second substrate; and

a third surface of the first substrate opposite to the first surface and the second surface of the second substrate are disposed to oppose each other.

4. (Currently Amended) The interconnect substrate as defined in claim 3,

wherein a plurality of through-holes are formed in the first substrate, and the first interconnect pattern and the second interconnect pattern are electrically connected via the through-holes by the conductive material.

5. (Currently Amended) The interconnect substrate as defined in claim 4, wherein:

the first interconnect pattern passes over the through-holes;

the through-holes are positioned over the second interconnect pattern; and

~~a~~ the conductive material contacting the first and second interconnect pattern

is provided within the through-holes.

6. (Withdrawn) The interconnect substrate as defined in claim 4, wherein:

the through-holes are positioned over the second interconnect pattern; and

a part of the first interconnect pattern enters the through-holes, and is connected to the second interconnect pattern.

7. (Original) The interconnect substrate as defined in claim 4, wherein a plurality of through-holes are formed in the second substrate, for the formation of a plurality of external terminals electrically connected to the second interconnect pattern and projecting from a surface of the second substrate opposite to the surface on which the second interconnect pattern is formed.

8. (Original) The interconnect substrate as defined in claim 7, wherein the through-holes formed in the first substrate and the through-holes formed in the second substrate are formed in communicating positions.

9. (Withdrawn) The interconnect substrate as defined in claim 8, wherein a part of the second interconnect pattern enters the through-holes formed in the first substrate, and is connected to the first interconnect pattern.

10. (Withdrawn) The interconnect substrate as defined in claim 8, wherein a part of the first interconnect pattern and a part of the second interconnect pattern project from a surface of the second substrate via the through-holes formed in the second substrate and form external terminals.

11. (Withdrawn) The interconnect substrate as defined in claim 8, wherein a part of the second interconnect pattern projects into the through-holes formed in the second substrate, avoiding contact with the first interconnect pattern.

12. (Withdrawn and Previously Presented) The interconnect substrate as defined in claim 1, wherein the first and second substrates are adhered by an anisotropic conductive film including conductive particles.

13. (Withdrawn) The interconnect substrate as defined in claim 12, wherein the first and second interconnect patterns are electrically connected by the conductive particles.

14-39. (Cancelled)

40. (Previously Presented) The interconnect substrate as defined in claim 1, further comprising:

an adhesive disposed between the first and second substrates.

41. (Previously Presented) The interconnect substrate as defined in claim 5, wherein the conductive material projects from the third surface of the first substrate.